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Examiner: Hicham B. Foud **Group:** 2419

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Applicant: David E. Jones

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Comments:

Attached please find a document for your review and consideration, in preparation for our telephone interview on June 11, 2009.

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PATENT APPLICATION
Attorney's Docket No.: 2037.1010-002

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	David E. Jones		
Application No.:	10/614,558	Group:	2419
Filed:	July 7, 2003	Examiner:	Hicham B. Foud
Confirmation No:	5801		
For:	METHOD AND APPARATUS FOR PROVIDING A PACKET BUFFER RANDOM ACCESS MEMORY		

CERTIFICATE OF MAILING OR TRANSMISSION

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INFORMAL DOCUMENT FOR EXAMINER INTERVIEW

Sir:

This Informal Document is being submitted in anticipation of a telephone interview with the Examiner scheduled for June 11, 2009, at 2:00 PM EST. Applicant looks forward to discussing the proposed claim amendments and remarks provided below.

Amendments to the Claims

Please amend Claims 1 and 7. The Claim Listing below will replace all prior versions of the claims in the application:

Claim Listing

What is claimed is:

1. (Currently amended) A packet buffer random access memory (PBRAM) device, comprising:

(a) a memory array;

(b) a plurality of input ports to be coupled to a network controller device, the memory array for storing packet data received by the plurality of input ports being shared by the plurality of input ports; and

(c) a plurality of serial registers each associated with a different one of the plurality of input ports, each of the serial registers configured for receiving packet data from the associated input port at a segment of a serial register concurrent with writing other packet data to the memory array [[at]] from another segment of the serial register, each of the serial registers further being segmented into a plurality of segments, segments of respective serial registers being associated with corresponding portions of the memory array, segments of different serial registers simultaneously transferring packet data to different portions of the memory array.

2. (Original) The PBRAM device of claim 1 wherein packet data is transferred into one segment of a serial register as data is simultaneously transferred out of another segment of the serial register.

3. (Original) The PBRAM device of claim 1 wherein a portion of the memory array is a queue.

4. (Original) The PRAM device of claim 3 wherein the queue includes a plurality of sub-queues, each sub-queue assigned a priority level.

5. (Original) The PBRAM device of claim 4 wherein packet data is read from the sub-queue with the highest priority level that stores data.

6. (Original) The PBRAM device of claim 1 wherein the memory array is a single global memory.

7. (Currently amended) A method for storing data packets transferred across a computer network in a packet buffer random access memory (PBRAM) device, the method comprising:

receiving a plurality of data packets from controllers coupled to said computer network at a plurality of input ports of the PBRAM device;

serially transferring portions of the data packets to different segments of serial registers that are connected between the input ports and a memory array, each of the serial registers being associated with a different one of the input ports, the memory array for storing packet data received by the input ports being shared by the plurality of input ports; and

conveying the portions of the data packets from one of the serial registers to different portions of the memory array in parallel, while concurrently transferring other portions of the packets to other segments of the one of the serial registers.

8. (Original) The method of claim 7 wherein a portion of the memory array is a queue.

9. (Original) The method of claim 8 wherein the queue includes a plurality of sub-queues, each sub-queue assigned a priority level.

10. (Original) The method of claim 9 wherein packet data is read from the sub-queue with the highest priority level that stores data.

11. (Original) The PBRAM device of claim 7 wherein the memory array is a single global memory.

12. (Previously presented) A packet buffer random access memory (PBRAM) device comprising:

a memory array;

a plurality of input ports coupled to the memory array by serial registers for conveying data to the memory array, each of the serial registers being associated with a different one of the input ports and configured for receiving packet data from the associated input port to a segment of a serial register concurrent with writing other packet data to the memory array from another segment of the serial register, the memory array for storing packet data received by the plurality of ports being shared by the plurality of input ports;

a plurality of command ports for receiving commands that indicate desired operations to be performed in relation to the data conveyed on the input ports; and

a memory management unit coupled between the command ports and the memory array, said memory management unit establishing input queue structures within the memory array responsive to write commands issued on the command ports, the input queue structures for receiving pointers to locations in a packet table that point to the data that is conveyed from the input ports.

13. (Original) The PBRAM device of claim 12 wherein the memory array is a single global memory.

14-17. (Cancelled)

18. (Previously presented) An apparatus for storing packets transferred across a computer network in a packet buffer random access memory (PBRAM) device, comprising:

means for receiving a plurality of packets from controllers coupled to said computer network by a plurality of input ports of the PBRAM device;

means for assigning input queue structures, contained in a memory array portion of the PBRAM device, to store packets, the memory array being shared by the plurality of input ports;

means for serially transferring portions of the packets to different segments of serial registers that are connected to the input ports and to the memory array, each of the serial registers associated with a different one of the input ports;

means for conveying the portions of the packets from a segment of a serial register to the memory array portion in parallel, concurrent with receiving other packet data to another segment of the serial register; and

means for storing said packets in said queue structures, said queue structures being further accessible by a plurality of output ports of said PBRAM device such that said input queue structures become output queue structures that deliver the packets to associated output ports.

19. (Original) The apparatus of claim 18 wherein an output queue structure includes a plurality of sub-queues, each sub-queue assigned a priority level.

20. (Original) The apparatus of claim 19 wherein packet data is read from the sub-queue with the highest priority level that stores data.

21. (Original) The PBRAM device of claim 18 wherein the means for storing is a single global memory.

22-25. (Cancelled)

REMARKS

Claims 1-13 and 18-21 are pending in this Application, of which claims 1, 7, 12 and 18 are the independent claims. All claims stand rejected.

Claim 1 is being amended to correct an obvious drafting error. Acceptance is respectfully requested.

Claim 7 is being amended to further clarify the scope of the invention. Acceptance is respectfully requested.

Rejection of claims 1-13 and 18-21 under 35 U.S.C. § 103

Claims 1, 2, 6, 7, 11-13, 18 and 21 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Toda et al. (U.S. Patent No. 5,612,925) in view of Turner (U.S. Patent No. 5,475,680). Claims 3-5, 8-10, 19 and 20 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Toda in view of Turner and further in view of Zuravleff et al. (U.S. Patent No. 5,867,735). Applicants respectfully disagree with these rejections for the reasons set forth below.

Claim 1 is directed to a packet buffer random access memory (PBRAM) device. Without limitation of the claims, an example PBRAM device is illustrated in Fig. 7, where the PBRAM device 62 includes a memory array 74, a plurality of input ports 70 (I/O Port 0 – I/O Port 31), and a plurality of serial registers 72 associated with the input ports 70 (serial register 0 – serial register 31). The serial registers 72 each receive packet data from one of the associated ports 70 and write the packet data to the memory array 74 (see Specification, page 4, lines 3-11). Each of the serial registers 72 is further segmented into a plurality of segments, each segment being associated with corresponding portions of the memory array 74. Such a configuration is illustrated in Fig. 8, where a serial register 72 is divided into segments of 256 bits each. Further, a segment of the serial register 72 may transfer data into the memory 74 concurrent with another segment of the serial register 72 receiving other data (page 13, lines 11-15). Claims 1, 12 and 18 are being amended as described above to further clarify this feature.

Toda discloses a memory device for transferring data to and from a memory. As shown in Fig. 16, the memory device 161 includes a memory cell 162, a serial register 167 (the label

"164" is a typographical error; see col. 12, lines 25-28), and a data I/O port 164. The serial register 167 has 8 bits. During a typical write operation, data received at the I/O port is transferred serially into the serial register 167. Once an address of the memory cell 162 is selected, the serial register 167 transfers the 8 data bits simultaneously into the memory cell at the selected address (col. 12, lines 17-33).

Toda fails to disclose "a plurality of input ports," where a "memory array...[is] shared by the plurality of input ports," as recited in Claim 1. As shown in Fig. 16, Toda discloses only a single I/O port 164, and does not teach or suggest additional ports for storing data to the memory cell 162. Toda's failure to teach "a plurality of input ports" was pointed out in two previous Amendments (*see* Amendment filed June 28, 2007, pages 9-10; and Amendment filed December 3, 2007, page 8). As a result of Applicant's previous remarks, a § 102 rejection of Claim 1 with regard to Toda was withdrawn, and a subsequent Office Action relied instead on Joffe (U.S. Patent No. 5,440,523) for the teaching of "a plurality of input ports" (*see* Office Action mailed February 5, 2008, page 3). Though Joffe is no longer relied upon, Toda still fails to disclose or suggest "a plurality of input ports" as recited in Claim 1.

The Office Action states that Toda fails to disclose 1) "a plurality of serial registers each associated with a different one of the plurality of input ports," and 2) "each of the serial registers [being] configured for receiving packet data from the associated input port at a segment of a serial register concurrent with writing other packet data to the memory array at another segment of the serial register," as recited in Claim 1. Applicant agrees. However, Turner, on which the Examiner relies for those features, also fails to suggest at least some of the aforementioned features.

Turner discloses an asynchronous time division multiplex (ATDM) switching system. As shown in Fig. 4, Turner receives data packets via 16 serial input lines 107 to a serial-to-parallel converter 100. The converter 100 includes two shift registers for each input line, where each shift register stores one half of a packet received at the respective input line (col. 3, line 58 – col. 4, line 8). These two packet halves, referred to as "A halves" and "B halves," are then transferred from the shift registers into separate blocks of RAM, "A Data" RAM 101 and "B Data" RAM 102, respectively (col. 4, lines 5-15).

Turner fails to disclose "serial registers configured for receiving packet data from the associated port at a segment of a serial register concurrent with writing other packet data to the memory array from another segment of the serial register" as recited in amended Claim 1. Turner does state that one register (e.g., the "A data" register) can transfer data to a respective RAM block at the same time that another register (e.g., the "B data" register) is loaded with data from the input port (col. 4, lines 8-15). Yet the "A data" and "B data" registers are not segments of a single serial register. Rather, they are individual shift registers, and each receives a half of an incoming packet (col. 3, line 64 – col. 4, line 8). Turner does not teach or suggest configuring either an "A data" or "B data" register for receiving packet data to one segment of a register concurrently with writing other packet data from another segment of the register. For at least the reasons above, Turner fails to disclose the "serial registers" as recited in Claim 1. Accordingly, even a combination of the references does not teach all elements of the claims.

Amended Claim 7 and Claims 12 and 18 recite features comparable to those described above with respect to Claim 1, and so are not anticipated nor made obvious by Toda and Turner. Claims 2, 6, 11, 13 and 21 depend from one of claims 1, 7, 12 and 18 and so inherit the features described above. Due to the aforementioned shortcomings of Toda and Turner, no combination of Toda, Turner and Zuravleff render obvious the invention as recited in Claims 3-5, 8-10, 19 and 20. As a result, the § 103 rejection of Claims 1-13 and 18-21 is believed to be overcome, and reconsideration is respectfully requested.

CONCLUSION

In view of the above amendments and remarks, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned.

Respectfully submitted,

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